CLAIMS

What is claimed is:

1) A circuit for measuring on-chip cycle-to-cycle jitter comprising:

a) a programmable delay line with an input, an output, and control inputs;

b) a programmable phase comparator with a first input, a second input, a programming input, a first output, and a second output;

c) a first counter with an input and an output;

d) a second counter with an input and an output;

e) wherein a clock signal is connected to the input of the programmable delay line and to the first input of the programmable phase comparator;

f) wherein the delayed clock signal of the programmable delay line is connected to the second input of the programmable phase comparator;

g) wherein the first output of the programmable phase comparator is connected to the input of the first counter;

h) wherein the second output of the programmable phase comparator is connected to the input of the second counter;

i) such that the first counter counts the number of times the time difference between the period of the clock signal and the period of delayed clock signal is a positive value larger than a dead zone value programmed by the programmable phase comparator;

j) such that the second counter counts the number of times the time difference between the period of the clock signal and the period of the

delayed clock signal is a negative value whose absolute value is larger than a dead zone value programmed by the programmable phase comparator.

2) A circuit as in Claim 1 wherein the programmable delay line comprises:

a) an inverter chain with an input and output;

b) a multiplexer with multiple inputs, control inputs, and an output;

c) wherein each input of the multiple inputs of the multiplexer is connected to a separate individual node of the inverter chain;

d) wherein the input of the inverter chain is the input of the programmable delay line;

e) wherein the output of the multiplexer is the output of the programmable delay line;

f) such that the delay of the programmable delay line may be fine tuned by selecting one of the multiple inputs of the multiplexer using the control inputs of the multiplexer.

3) A circuit as in Claim 1 wherein the programmable delay line comprises:

a) a first inverter chain with an input and output;

b) a second inverter chain with an input and output;

c) a first multiplexer with multiple inputs, control inputs, and an output;

d) a second multiplexer with multiple inputs, control inputs, and an output;

e) wherein each input of the multiple inputs of the first multiplexer is connected to a separate individual node of the first inverter chain;

f) wherein each input of the multiple inputs of the second multiplexer is connected to a separate individual node of the second inverter chain;

g) wherein the input of the first inverter chain is the input of the programmable delay line;

h) wherein the output of the second multiplexer is the output of the programmable delay line;

i) wherein the output of the first multiplexer is connected to the input of the second inverter chain;

j) such that the delay of the programmable delay line may be fine tuned by selecting one of the multiple inputs of the first multiplexer and second multiplexer using the control inputs of the first multiplexer and second multiplexer.

4) A circuit as in Claim 3 wherein the time delay through any individual inverter in the first inverter chain is shorter than the time delay through any individual inverter in the second inverter chain.

5) A circuit as in Claim 3 wherein the time delay through any individual inverter in the first inverter chain is longer than the time delay through any individual inverter in the second inverter chain.

6) A circuit as in Claim 1 wherein the programmable delay line comprises:

a) a first inverter chain with an input and output;

b) a second inverter chain with an input and output;

c) a first multiplexer with multiple inputs, control inputs, and an output;

d) a second multiplexer with multiple inputs, control inputs, and an output;

e) a set of NFETs;

f) a set of capacitors;

g) a set of control signals;

h) wherein each input of the multiple inputs of the first multiplexer is connected to a separate individual node of the first inverter chain;

i) wherein each input of the multiple inputs of the second multiplexer is connected to a separate individual node of the second inverter chain;

j) wherein the input of the first inverter chain is the input of the programmable delay line;

k) wherein the output of the second multiplexer is the output of the programmable delay line;

l) wherein the output of the first multiplexer is connected to the input of the second inverter chain;

m) wherein the drain of each NFET in the set of NFETs is connected to the output of the programmable delay line;

n) where in the gate of each NFET in the set of NETs is connected to an individual control signal in the set of control signals;

o) where in the source of each NFET in the set of NETs is connected to an individual first connection of each capacitor in the set of capacitors;

p) where in each second connection to each capacitor in the set of capacitors is connected to ground;

q) such that the delay of the programmable delay line may be fine tuned by selecting one of the multiple inputs of the first multiplexer using the control inputs of the first multiplexer and;

r) the delay of the programmable delay line may be fine tuned by selecting one of the multiple inputs of the second multiplexer using the control inputs of the second multiplexer and;

s) the delay of the programmable delay line may be fine tuned by selecting an appropriate number of capacitors from the set of capacitors using an appropriate combination of the control signals from the set of control signals connected to the set of NFETs.

7) A circuit as in Claim 6 wherein the time delay through any individual inverter in the first inverter chain is shorter than the time delay through any individual inverter in the second inverter chain.

8) A circuit as in Claim 6 wherein the time delay through any individual inverter in the first inverter chain is longer than the time delay through any individual inverter in the second inverter chain.

9) A circuit as in Claim 6 wherein the resolution of the fine-tuning achieved by selecting the appropriate control signals is smaller than the resolution needed to measure on-chip, cycle-to-cycle jitter.

10) A circuit as in Claim 1 wherein the time difference between the period of the clock signal and the period of the delayed clock signal is measured from the positive-going zero-crossing of the clock signal to the positive-going zero-crossing of the delayed clock signal.

11) A method for measuring cycle-to-cycle jitter on chip comprising:

a) fabricating a programmable delay line;

b) fabricating a programmable phase comparator;

c) fabricating a first counter;

d) fabricating a second counter;

e) connecting a clock signal to an input of the programmable delay line and to a first input of the programmable phase comparator;

f) connecting a delayed clock signal from the programmable delay line to a second input of the programmable phase comparator;

g) connecting a first output from the programmable phase comparator to an input of the first counter;

h) connecting a second output from the programmable phase comparator to an input of the second counter;

i) programming the programmable delay line to produce the delayed clock signal such that the delayed clock signal is one clock cycle delayed from the clock signal;

j) programming the programmable phase comparator to measure the time difference between the period of the clock signal and the period of the delayed clock signal;

k) programming a dead zone for the programmable phase comparator;

l) such that if the time difference between the period of the clock signal and the period of the delayed clock signal is greater than the dead zone, the first counter is triggered;

m) such that if the time difference between the period of the clock signal and the period of the delayed clock signal is negative and the absolute value is greater than the dead zone, the second counter is triggered;

n) wherein the values in the first and second counters are used to determine a statistical distribution;

o) wherein the statistical distribution is used to determine on-chip, cycle-to-cycle jitter.

12) A method as in Claim 11 wherein measurements are made at more than one location on a clock distribution.

13) A method as in Claim 11 wherein the statistical distribution is gaussian.

14) A method as in Claim 11 wherein the programmable delay line comprises:

a) an inverter chain with an input and output;

b) a multiplexer with multiple inputs, control inputs, and an output;

c) wherein each input of the multiple inputs of the multiplexer is connected to a separate individual node of the inverter chain;

d) wherein the input of the inverter chain is the input of the programmable delay line;

e) wherein the output of the multiplexer is the output of the programmable delay line;

f) such that the delay of the programmable delay line may be varied by selecting one of the multiple inputs of the multiplexer using the control inputs of the multiplexer.

15) A method as in Claim 11 wherein the programmable delay line comprises:

a) a first inverter chain with an input and output;

b) a second inverter chain with an input and output;

c) a first multiplexer with multiple inputs, control inputs, and an output;

d) a second multiplexer with multiple inputs, control inputs, and an output;

e) wherein each input of the multiple inputs of the first multiplexer is connected to a separate individual node of the first inverter chain;

f) wherein each input of the multiple inputs of the second multiplexer is connected to a separate individual node of the second inverter chain;

g) wherein the input of the first inverter chain is the input of the programmable delay line;

h) wherein the output of the second multiplexer is the output of the programmable delay line;

i) wherein the output of the first multiplexer is connected to the input of the second inverter chain;

j) such that the delay of the programmable delay line may be varied by selecting one of the multiple inputs of the first multiplexer and second multiplexer using the control inputs of the first multiplexer and second multiplexer.

16) A method as in Claim 11 wherein the time delay through any individual inverter in the first inverter chain is shorter than the time delay through any individual inverter in the second inverter chain.

17) A method as in Claim 11 wherein the time delay through any individual inverter in the first inverter chain is longer than the time delay through any individual inverter in the second inverter chain.

18) A method as in Claim 11 wherein the programmable delay line comprises:

a) a first inverter chain with an input and output;

b) a second inverter chain with an input and output;

c) a first multiplexer with multiple inputs, control inputs, and an output;

d) a second multiplexer with multiple inputs, control inputs, and an output;

e) a set of NFETs;

f) a set of capacitors;

g) a set of control signals;

h) wherein each input of the multiple inputs of the first multiplexer is connected to a separate individual node of the first inverter chain;

i) wherein each input of the multiple inputs of the second multiplexer is connected to a separate individual node of the second inverter chain;

j) wherein the input of the first inverter chain is the input of the programmable delay line;

k) wherein the output of the second multiplexer is the output of the programmable delay line;

l) wherein the output of the first multiplexer is connected to the input of the second inverter chain;

m) wherein the drain of each NFET in the set of NFETs is connected to the output of the programmable delay line;

n) where in the gate of each NFET in the set of NETs is connected to an individual control signal in the set of control signals;

o) where in the source of each NFET in the set of NETs is connected to an individual first connection of each capacitor in the set of capacitors;

p) where in each second connection to each capacitor in the set of capacitors is connected to ground;

q) such that the delay of the programmable delay line may be fine tuned by selecting one of the multiple inputs of the first multiplexer using the control inputs of the first multiplexer and;

r) the delay of the programmable delay line may be fine tuned by selecting one of the multiple inputs of the second multiplexer using the control inputs of the second multiplexer and;

s) the delay of the programmable delay line may be fine tuned by selecting an appropriate number of capacitors from the set of capacitors using an appropriate combination of the control signals from the set of control signals connected to the set of NFETs.

19) A method as in Claim 11 wherein the time difference between the period of the clock signal and the period of the delayed clock signal is measured from the positive-going zero-crossing of the clock signal to the positive-going zero-crossing of the delayed clock signal.